IN THE SPECIFICATION

Please amend the specification as follows.

The paragraph beginning at page 13, line 7 is amended as follows:

An example method [[200]] for performing component partitioning and allocation according to an implementation of the present invention is shown in FIG. 2. One goal commonly sought by partitioning a software system is to group the tasks and data blocks into *components* that are internally cohesive and have relatively low external couplings. An upper limit on component size is the capacity of the largest hardware unit available. The existence of even a few small components simplifies the allocation's bin-packing process.

The paragraph beginning at page 39, line 13 is amended as follows:

Figure 5 illustrates the tasks and peripherals, but also shows the data blocks and the data couplings, instead of the control and peripheral couplings. These two figures show separate views only for clarification, both sets of information are interleaved in the algorithmic process. ~~Figure 6~~ Figure 5 also adds in the directional dependencies (a *read* is shown as an arrow from data-block to task; a *write* is described as the reverse) between the tasks and the data blocks. A task that both reads and writes the same data block has two separate couplings, supporting the description of any differences in frequency, timing, or bandwidth.

The paragraph beginning at page 40, line 6 is amended as follows:

Table 10 shows the triples for this example, implemented as a set of three columns (control, data, and peripheral), and ten rows (values 1 - 10) representing the range of coupling strengths. In Table [[13]] 10, these thresholds (shown as double lines) are CT = 7, DT = 5, and PT = 3. In this example, [[thc]] the peripheral threshold has no direct impact in the algorithmic process, since the lowest peripheral coupling has a strength of 7.

The Table beginning at page 41, line 1 is amended as follows:

Table 10 Coupling Details

Strength	Control Couplings	Data Couplings	Peripheral Couplings
10		(Fl NI 10)(Al M1 10)	(Fore-Sonar F1 10) (Aft-Sonar Al 10)
9	(Aft-Sonar A3 9) (Aft-Sonar B1 9) (Al A2 9) (Fore-Sonar F3 9) (Fore-Sonar B1 9) (Fl F2 9)	(N1 F3 9) (B2 82 9) (M1 A3 9)(D2 TI 9)	(Fore:-Sonar B1 9) (Aft-Sonar B1 9)
8	(A2 A4 8) (A3 A4 8) (F2 F4 8) (F3 F4 8)	(B3 TI 8)	(Keyboard D 1 8)
7		(N3 B2 7)(M3 B2 7) (TI D3 7)	(D3 Display-1 7) (D3 Display-2 7)
6	(A4 B2 6) (B2 B3 6) (F4 B2 6) (D1 D3 6)	(M1 A2 6) (M2 A4 6) (S1 B3 6) (N1 F2 6) (N2 F4 6)	
5	(B1 B3 5) (B3 D1 5) (D3 B3 5)	(A3 M2 5) (F3 N2 5)	
4		(A4 M3 4)(B1 S1 4) (DI TI 4) (F2 N2 4) (A2 M2 4) (F4 N3 4)	
3		(S2 B3 3)	
2			
1			

The Table beginning at page 42, line 26 – page 43, lines 2 is amended as follows:

Table 12 Initial Platform Loads

Platform (Component)	**Processor** Capacity	**Processor** Utilization	Memory Capacity	Memory **Utilization**
P1 (C4)	15 mips	68%	300 mb	84%
P2 (C3 &C5)	60 mips	93%	200 mb	88%
P3 (C1)	70 mips	89%	1 gb	90%
P4 (C2)	50 mips	~~90%0~~ 90%	I gb	80%

The Table beginning at page 43, line 14 is amended as follows:

Table 13 Modified Platform Loads

Platform (Component)	Processor Capacity	Processor Utilization	Memory Capacity	Memory Utilization
Px (C3, C4 & C5)	80 mips	82%	600 mb	~~71"~~ 71%
P3 (C11)	70 mips	86%	1 gb	80%
P4 (C2)	50 mips	~~900~~ 90%	1 gb	90%

The paragraph beginning at page 37, line 20 is amended as follows:

FIG. 4 shows an exemplary system that comprises four computers, with a functional partitioning and allocation into four components:

1. Sonar software (processing data from the Fore sensors), Tasks F_1-F_4 in FIG. 4,
2. Sonar software (processing data from the Aft sensors), Tasks A_1-A_4 ~~n FIG. 4~~ in FIG. 4,
3. Bearing Tracker software, Tasks B_1-B_3 in FIG 4, and
4. Display software, Tasks D_1-D_4 in FIG. 4.